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ENDING DECEMBER 31, 1973

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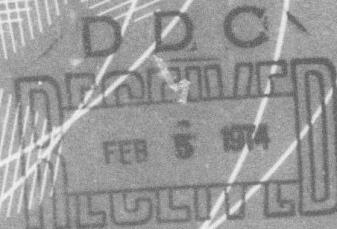
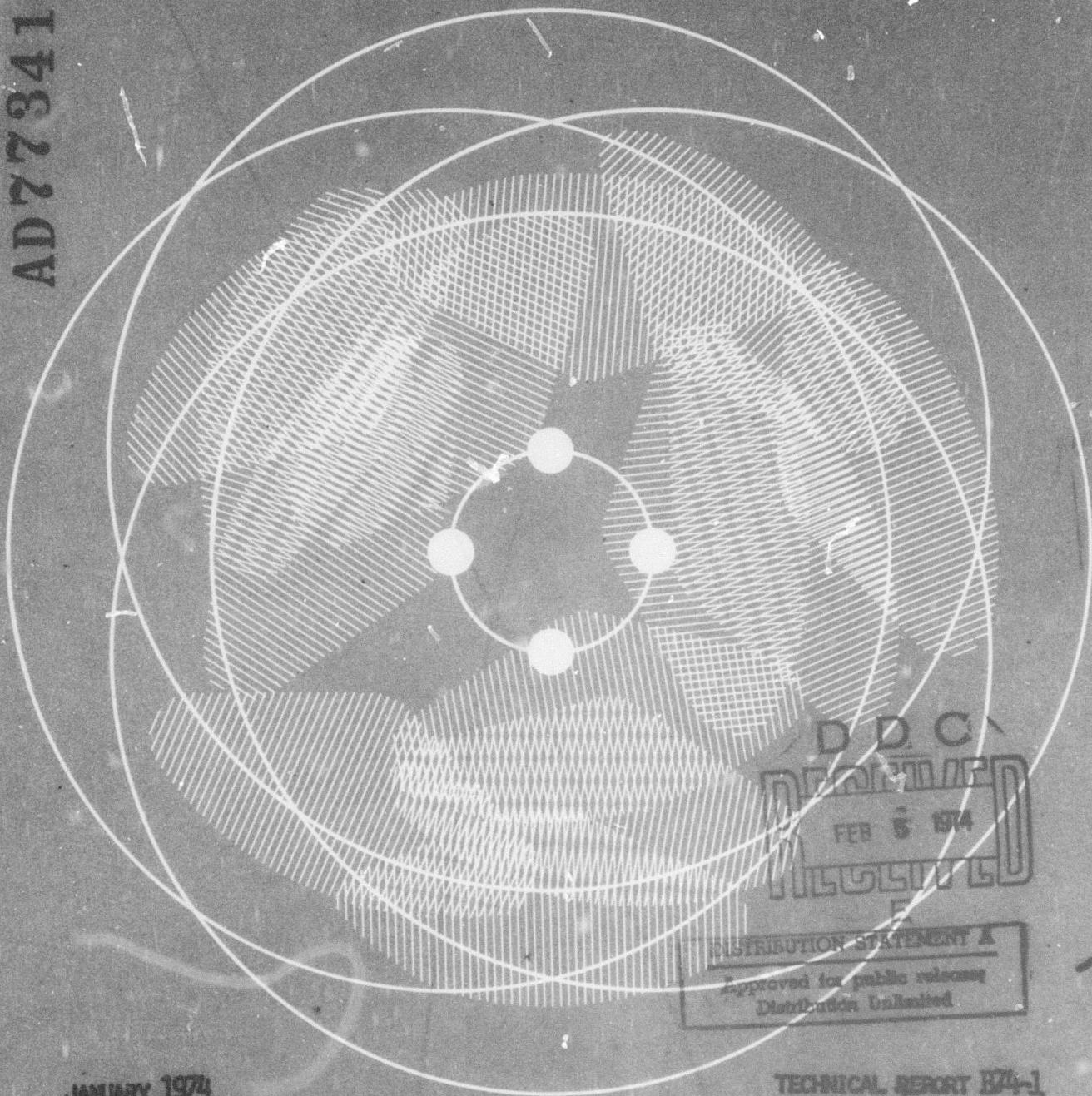


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ANNUAL TECHNICAL REPORT

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TECHNICAL REPORT E4-1

THE ALOHA SYSTEM
UNIVERSITY OF HAWAII
HONOLULU, HAWAII 96822

ANNUAL TECHNICAL REPORT

Year Ending Dec. 31, 1973

ARPA Order Number 1956

Program Code Number 2P10

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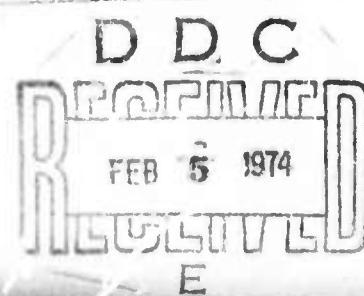
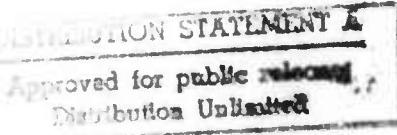
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Short Title of Work: THE ALOHA SYSTEM

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SUMMARY

Our work in THE ALOHA SYSTEM is divided into two tasks:

Task I: To develop new methods and protocols for random access radio communications for computers;

Task II: To study systematic designs for multiprocessor computing structures through the developments of the BCC 500 system.

We will discuss the accomplishments by task.

TASK I

The work in Task I is divided between radio (ground) and satellite communications.

Radio Communications: In this area our primary work was part of the overall effort of the Packet Radio Group under the direction of R. E. Kahn of ARPA. Our accomplishments were in the following areas:

1. *Theoretical Studies.* New results were derived on the spatial capacity of a random access (ALOHA) channel in the presence of perfect capture. A second study was completed comparing the thruputs of spread spectrum versus ALOHA multiplexing techniques.

2. *Simulation Studies.* A study was completed comparing the advantages of negative and positive acknowledgement schemes in a packet radio environment.

This study is part of an extensive simulation effort which is nearing completion in which we have put together a minicomputer facility which will allow validation and data collection for different channel organizations.

3. *Radio System Studies.* During 1973 radio system studies were undertaken which were composed of measurements of certain channel and source characteristics of the ALOHA packet radio facility and investigations of modulation methods and

antenna configurations for packet radio configurations.

4. *Packet Radio Test Facility.* The major design effort in 1973 was to design and build a packet radio repeater. With the repeater operating successfully, interisland communications on the ALOHA radio net became possible for the first time. Another important design effort was the design and implementation of a programmable terminal control unit (TCU) involving an INTEL 8008 microcomputer on a single integrated circuit chip. This integrated TCU serves as a model for the Packet Radio Group.

Satellite Communications: In satellite communications we have been involved in a joint study with ARPA, BBN and UCLA to investigate the theory and to design the protocols for packet communications via broadcast satellite. These studies have been very fruitful for ALOHA researchers and are described in a series of ARPANET Satellite System Notes 22, 26, 29, 30, 32, 36 and 37. In the second satellite project we are involved in, we are developing a small ground station for experimenting with the NASA satellite ATS-1 on a broadcast mode. We have designed and built equipment for the ground station which are based on the original ALOHA SYSTEM hardware. A prototype ground station is in operation, and a random access burst channel is now in operation between Honolulu, and NASA/Ames. Shortly we will be connected Alaska, Japan, Australia, and New Zealand.

TASK II

Almost all of the Task's efforts were directed towards completion and expansion of the BCC 500 computer hardware and software.

Most of the hardware of the 500 has been rebuilt or refurbished with faster, more reliable circuitry. Documentation proceeded in parallel and by the end

of 1973, both hardware and documentation were in a good state, and the system was usable on a limited basis.

The major task of the software group was to debug the language SPL and then to rewrite and recompile the operating system using this refurbished and more robust version of SPL.

A Network Control Program was written entirely in microcode to be run on one of the 500 microprocessors. This is a new innovation inasmuch as most of the ARPANET's NCP's have been implemented in software only.

A new microprocessor was designed to function as a communications controller for the ILLIAC System.

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RESEARCH PROGRAM

The research program of THE ALOHA SYSTEM is twofold:

Task I - to develop new methods of random access radio communications for computer systems, and to define those situations where radio communications provides a reasonable alternative to conventional computer communication techniques. In addition, to study packet communications techniques using satellites.

Task II - to develop more effective means for inter-computer communication and more organized, systematic designs for multiprocessor computing structures with special emphasis on the security aspects of multiprocessor systems; to operate the BCC 500 multiprocessor computing system for use by the ALOHA communication net and the ARPA network.

We will describe the technical accomplishments of the project by task.

TECHNICAL RESULTS (TASK I)

Radio Communications

Introduction: Developments in remote access computing during the latter part of the 1960's have resulted in increasing importance of remote time-sharing, remote job entry and networking for large information processing systems. The present generation of computer-communication systems is based on the use of leased or dial-up common carrier facilities, primarily wire connections. Under many conditions such communication facilities offer the best possible communications option to the overall system designer of a large computer-communication facility. In other circumstances, however, the organization of

common carrier data communication systems seriously limits the possibilities of a large information processing system.

When the constraint of data communications by wire is eliminated a number of options for different methods of organizing data communications within a computer-communications net are made available to the system designer. THE ALOHA SYSTEM project has investigated the use of a new and simple form of random access communications for a statewide university computing system; the first links in this UHF radio-linked computer system were set up in 1971.

Since that time THE ALOHA SYSTEM has been in continuous operation. The ALOHA network uses two 24,000 baud channels at 407.350 MHz and at 413.475 MHz in the upper UHF band. ALOHA uses packet switching techniques similar to that employed by the ARPANET, in conjunction with a novel form of random-access radio-channel multiplexing.

Packet Radio: Most of THE ALOHA SYSTEM's work in radio communications in 1973 was part of the Packet Radio Project under the direction of R. E. Kahn of ARPA/IPT. The objective of the Project is to investigate the feasibility of establishing a store and forward radio communications net with many of the features of the ARPA and ALOHA networks. At present the Packet Radio Group consists of representatives from ARPA, Network Analysis Corporation, Stanford Research Institute, UCLA, Bolt Beranek and Newman, Collins Radio and ALOHA.

Since THE ALOHA SYSTEM is the only operational radio communications system of the Group, its role in the Packet Radio effort had special significance. In 1973, THE ALOHA SYSTEM served as an experimental test facility in which research issues of immediate concern to the Packet Radio Group could be studied in a real user environment. The principal issues which were studied

by ALOHA were:

A. Theoretical Studies

Norman Abramson and N. Thomas Gaarder derived some new results on the spatial capacity of an ALOHA channel in the presence of perfect capture. These results are discussed in Packet Radio Temporary (PRT) Notes #49 and #60 [1,2].

Parimi Murthy has done a study comparing the throughputs of spread-spectrum and ALOHA multiplexing techniques [3]. This study is important inasmuch as the Packet Radio Group has decided to implement its preliminary system with spread spectrum techniques. THE ALOHA SYSTEM is continuing to use the ALOHA random access technique so that there will be two parallel systems to be compared and evaluated.

B. Simulation Studies

Richard Binder and Lee Castonguay have done a system study comparing the advantages and disadvantages of negative and positive acknowledgement schemes in a packet radio environment. The work is reported in PRT Note #44 [4]. This study is part of an extensive simulation effort which is nearing completion in which we have put together a minicomputer facility which will allow validation and data collection for different channel organizations. The facility is a three CPU multiprocessor and will initially run a channel simulator program and channel controller (MENEHUNE) station program in conjunction with a user simulator program that will allow loading of a channel with hundreds of simulated data sources, allowing real-time verification of channel behavior under loaded conditions. As of this moment the channel simulator and channel controller software is finished and we are still working on the user simulator

programs. This study has taken longer than anticipated due to late delivery and malfunctioning of the Lockheed SUE minicomputer hardware. A paper has been presented at the 1973 Asilomar Conference discussing the planning and objectives of the simulation study [5].

C. Radio System Studies

During 1973 radio system studies were undertaken which were composed of measurements of certain channel and source characteristics of the ALOHA packet radio facility and investigations of modulation methods and antenna configurations for packet radio communications.

In particular, a measurement program for loss of field strength for the ALOHA channel has been completed. The measurements were made at 413 MHz over various situations of elevation and environment in Oahu. The collected data were then analyzed statistically. The results, given in PRT Note #70 [6], confirm the importance of performing radio range measurements for packet radio transmission.

Another set of measurements that were undertaken concerned impulse noise and its effect upon the burst communication ALOHA channel. Time domain statistics were obtained on impulse noise occurrences and received impulse noise power levels at selected receiver locations. The results were analyzed statistically on the IBM 360/65 computer and are detailed in PRT Note #50 [7].

Other measurements that are continuing involve radio field strength, FM capture effects, packet error-rate and throughput. These and other measurements are being coordinated with the SRI Group under Stanley Fralick who has the primary responsibility for radio range measurements for the Packet Radio Group.

D. Packet Radio Test Facility

During 1973 a primary effort of ALOHA was to design and build a packet radio repeater. Since the transmission scheme of the operational ALOHA network is by line-of-sight, repeaters are necessary to operate in an environment such as Honolulu where a diversity of terrain (mountains, high-rise buildings, heavy foliage, etc.) severely limits the radio range.

A preliminary version of the ALOHA packet repeater has been built and debugged. Preliminary tests in Oahu indicates that the repeater functions as designed. In early January 1974, tests will be made from Mount Haleakala in Maui to test the range of the repeater and the effects of radio interference upon its operation.

A second project which we have strongly emphasized is the design of a integrated terminal control unit (TCU) which is the major communication module at the terminal end of the ALOHA net. Present hard-wire versions are bulky and expensive. Thus we have concentrated on the development of a new TCU involving an INTEL 8008 microcomputer on a single integrated circuit chip. The TCU-on-a-chip will enable the system to respond to a variety of different transmission protocols, including variable length packets and character-by-character transmission. A preliminary version of the TCU-on-a-chip has just been completed and the software is undergoing final stages of debugging. The job is on ongoing project and many of the experimental protocols are yet to be implemented.

Satellite Communications

Introduction: Because of the geographic isolation of Hawaii, one of the original objectives of THE ALOHA SYSTEM project was to study the feasibility of computer

communications by means of satellite. With the development of digital communication systems by COMSAT in which data at the rate of 50K baud can be transmitted through a single voice channel data transmission by satellite has become both technologically and economically feasible.

There is a basic and important difference between the use of a satellite channel and a wire channel for data communications. The satellite channel is a broadcast channel as opposed to a point-to-point wire channel, so that a single voice channel, say between ground stations A and B can be used in broadcast mode among any set of ground stations, providing a full broadcast capability of two 50K baud channels. Thus a single commercial satellite voice channel could be employed with the following characteristics: (1) The single voice channel could provide two up-link and two down-link 50K baud data channels. (2) Each of these four channels could be simultaneously available to any COMSAT ground station in sight of the satellite.

ARPANET Satellite System: During the past year we have initiated two specific research projects for satellite extension of THE ALOHA SYSTEM and several theoretical studies involving the unique properties of satellite channels. The first of the projects involves the use of large commercial ground stations and the establishment of an ARPANET Satellite System; the second involves the use of small inexpensive ground stations in a joint research effort with NASA/AMES. In regard to the ARPANET Satellite System, we have been involved in a joint study with ARPA, Bolt Beranek and Newman, and UCLA to design a suitable protocol for packet communications via satellite. These studies have been very fruitful and are described in a series of ARPANET Satellite System (ASS) Notes #22, 26, 29, 30, 32, 36, and 37 [8-14].

ATS-1; The second satellite project involves the use of the NASA satellite ATS-1 using small, inexpensive ground stations, which cost less than \$5,000 each. Thus far we have progressed to the point where a random access burst mode data channel is in operation between the University of Hawaii and NASA/AMES Research Center in California. Early in 1974 this network will be joined by the University of Alaska.

In order to simplify and reduce the cost of the digital interface between the ATS-1 ground station radio transceiver and the digital equipment (TCU or Encoder-Decoder), it was decided to try a modified version of the ALOHA-designed modem in place of the set of equipment designed and supplied by NASA/AMES. The equipment supplied by NASA/AMES (other than the radio) consists primarily of a PCM Bit Synchronizer, a NASA-built Formatter/Synchronizer, and a Convolutional Coder/Decoder. This equipment, taken together, represents an investment in the order of \$10,000.00. By going to a block code and implementing the error correction function in software, the cost of the stand-alone coder/decoder could be saved. A standard 9.6 KBPS ALOHA modem was modified for rapid burst acquisition and low false-alarm rate. Minor modifications were made to the ATS-1 radio to interface the ALOHA modem and a simple interface unit was built to go between the modem and the radio. Tests to date have indicated the ALOHA modem arrangement to have about the same error rate capability as the NASA designed system. Therefore, the use of the cheaper ALOHA SYSTEM appears quite feasible. The cost of the ALOHA modem should be no more than \$500.00

TECHNICAL RESULTS (TASK II)

Design, Development, and Implementation of the BCC 500

Almost all of the Task's efforts were directed toward completion and expansion of the BCC 500 hardware and software obtained originally from Berkeley Computer Corporation. It should be recalled that this equipment and software were, while used somewhat by the company, substandard and incomplete. The first phase of the Task's work, therefore, was to refurbish the hardware and update and complete as much software as possible. This effort was originally projected to be accomplished within one and one-half years after the start of the Task.

The Task was unable to begin work for six months due to the lack of physical facilities, and due to the delay not as many former key BCC personnel were able to join the Task as originally projected, further slowing progress. Consequently, at the end of Year II the hardware was still not quite complete. The software work reflected a greater state of completion; however, documentation had not been done to an acceptable degree. Therefore at the end of the second year the main emphases of the Task were (a) to complete the hardware modifications as soon as possible and (b) to produce appropriate documentation to permit use of the system locally and to a lesser degree via the ARPA network.

A. BCC 500 Hardware

The following items and projects were worked on during the year:

1. CPU 1.5A

This CPU was refurbished and installed in the system during the year. It gave us a 40% increase in computing power over the slower CPU 1.0 when

it went into operation. The CPU is implemented as a microprocessor except that it is provided with a hardware multiplier, an instruction fetch unit, and a 128-entry memory map. The processor was the first one equipped with ROM parity. To do this required the production of updated and fully verified microcode source language and a number of programs to produce expanded listings with microcode including correct parity. The latter programs were useful for processing microcode for all other processors.

2. CPU 1.5B

The CPU was rebuilt and initial quality checked. There was no time during the year to bring up the processor and install it in the system.

3. CHIO

This processor was the only one which had been rebuilt and installed in the system last year. During the year several PC boards were replaced to permit the installation of ROM parity, new protects, new MPMBM, etc. The microcode was modified to permit concurrent operation of the CHIO and the common test processor (CTP), a portion of microcode emulating the instruction set of a processor similar to the Xerox 940. The new capability permits software to be executed on the CHIO to facilitate the ARPA network or other input-output not originally provided for in the CHIO.

4. Microscheduler (MSCH)

The processor was refurbished, installed in the system, provided with ROM parity and a number of other features to accommodate changes planned

but not yet made.

5. Auxiliary Memory Control (AMC)

This processor was similarly refurbished, installed in the system, provided with ROM parity, etc.

6. System Measurement Processor (SMP, or the CPU 1.0)

This processor is a standard BCC microprocessor with microcode to emulate a CPU fully. It is not as fast as a CPU 1.5. When the second CPU 1.5 is brought up, the processor will be free, i.e., it will not have any system duties. Thus it can be used to measure and monitor various aspects of system operation. For now it serves as a system backup to the CPU 1.5 and was so used on a number of occasions during the year when the faster processor failed. Such failures have diminished considerably as the CPU 1.5 now has "burned in".

7. Fast Memory (FM)

The Fast Memory is one of the more complex portions of the system and certainly one of the most crucial. It consists of four so-called "quadrants" of electronics connected to a total of eight Ampex core memory modules and serves to buffer and schedule memory requests from four conflicting sources over the eight core modules. In addition it contains a small amount of active storage giving a minor look-behind capability. The unit was refurbished and a number of design faults were noted and corrected. This resulted in the necessity for reconstruction of a small number of PC boards which was carried out during the year. The modifications were installed and checked out on one of the four quadrants. The other quadrants have as yet not been modified, as it was decided that

the entire Fast Memory backplane should be replaced in order to accommodate these modifications as well as an entirely new method for cabling and distributing the memory signals.

8. Microprocessor Memory Bus Multiplexer (MPMBM)

This device serves to multiplex the memory requests of the CHIO, MSCH, AMC, and SMP processors. It was merely installed in the system and brought up in an as-is condition, since it was determined that the memory cabling scheme used by BCC was unacceptable and would lead to unreliable system operation. The unit was redesigned, and a completely new cabling scheme with connectors was devised. There was no time during the year to build this equipment, although many modifications were made to accommodate it when it is built. All necessary materials were acquired.

9. Core Memory Modules

The Task received 11 Ampex RG core memory modules, each of 16K x 50 bit capacity, 1 usec cycle time. Several of these modules were not functional, as some deterioration of the electronics components had occurred. One had not yet been equipped with extensive modifications designed and installed by BCC. These modules were all placed in working condition, although they required and to a certain extent still require considerable attention.

10. Auxiliary Memory Transfer Unit (AMTU)

This unit contains all the drum/disk transfer and Fast Memory interface electronics. The unit is in poor condition but was installed and checked out without refurbishment. Total replacement would be

required to get the unit up to the standards of the rest of the system, and this was deemed impracticable because of the complexity of the unit. It was operated for nine months during the year with almost no failures.

11. Drum 0

The Bryant drum unit was received as a newly refurbished device from its manufacturer. It was placed into operation early in December 1972 on a temporary basis by the manufacturer's installer. Shortly thereafter it suffered a number of head crashes, taking out about 7% of the available storage area. Since it was not under warranty, it was up to Task II personnel to remedy the situation. Investigation showed that the crashes had occurred because of dirt within the drum chamber. Conjecture was that because of very dirty conditions in the room and of several possible means for entry of dirt in the unit, it would require complete cleaning every two months if it were ever to survive. Moreover, a drum that has experienced such an event seldom lives more than a few months afterward. A number of measures were then taken to forestall a major accident: The machine room was thoroughly cleaned and stern measures to keep it that way were instituted. Carpeting was installed on the floor and all personnel are required to remove their shoes upon entering the room, doing away with static electricity and reducing the amount of dirt brought into the room. A built-in vacuum cleaning system was installed so that dirt removed from the carpet was in no way transferred into the room atmosphere. The room was pressurized against dirt entry. The drum was sealed much more

carefully than the manufacturer sealed it. The unit was also pressurized with air passed through a micron filter and carefully dried. The method of cooling the unit was changed to eliminate the fans that were thought to be the major source for dirt entry. Finally the ruined heads were removed and a number of new heads installed. They, together with existing spares, made up for the loss of storage, and the drum was restored to full capacity. An aerosol particle detector was fitted to the unit. This proved invaluable in not only serving as a sentinel during operation of the unit but also as a means for locating heads which were not flying properly. All of this effort seemed to work. The unit functioned beautifully for the remainder of the year. Brief inspection indicates that over this time no noticeable dirt buildup occurred. This means that the unit may require servicing perhaps only every two years.

12. Drum 1

This unit was received originally in the equipment from BCC where it had run acceptably for months. However, it suffered the same fate as Drum 0. All of the measures devoted to Drum 0 left little time for dealing with Drum 1. The unit was cleaned up, the ruined heads removed, and a number of new heads installed but not flown. As the year ended we were approaching the completion of the repair but were awaiting a shipment of needed new heads.

13. Drum Electronics

As both drum units are 24 bit parallel devices, there is considerable electronics associated with them. For the most part this equipment was in

acceptable condition, requiring only cleaning and checking. Minor modification was made on some of the boards to improve signal quality.

14. Disk File

The disk file was completely rebuilt on site in Honolulu by Bryant personnel. A complete set of "crash-proof" disk surfaces was installed. During this time one of the two actuators failed and had to be replaced. The disk and its associated electronics began to perform acceptably, and during the year this performance was improved by occasional adjustments of various heads.

15. Protects

Analysis of the operation of the system revealed that the so-called "protects", a system of processor interlocks to permit the protection of system objects like global tables, were inadequate as implemented by BCC. This necessitated redesign of the entire system. The new design involved changes in all the processors as well as the production of four PC boards in the system Central Control area. Although the modifications to accommodate the protects were made during the year, the new mechanism could not be installed.

16. Maintenance Panel

A special panel was built with a number of lights to indicate various error or abnormal conditions within the system and a number of switches to permit various actions related to hardware maintenance.

17. Battery Charger

This unit works with a nickel-cadmium battery to provide a continuous source of power for a number of critical circuits in the system

such as the real-time clock. Minor rework and installation was accomplished.

18. Central Control

This unit was designed and built to replace equivalent BCC components which were clearly substandard. It contains clock generation and distribution and circuits used in conjunction with the maintenance panel.

19. CHIO Multiplexer -- Phase I

This unit was not refurbished, as it is intended eventually to replace it with an equivalent unit called Phase II. Some modification was required, however, to accommodate a connection to the ARPA network TIP. The unit is used to service 110 bps Teletypes and connect them with the CHIO processor.

20. Power Supplies

A number of power supply units (one for each unit in the system) were reconditioned and slightly modified. Each unit contains three commercial power supplies and a number of control and protection circuits. During the year a great number of problems were experienced with the commercial supplies. Mostly this is because of operation near the maximum load for each unit. A number of changes were required during the year to alleviate overloading and more properly distribute load.

21. Motor-Generator and Power Distribution

During the year the 37.5 KVA Motor-generator accompanying the BCC equipment was installed and placed in operation. The device removes all

switching transients from the primary power and provides for total voltage regulation. The motor and generator are connected to a one-ton flywheel which provides enough inertia to operate the generator for about 15 seconds after a primary power failure. Also, the primary power can fail for up to five seconds without forcing a shutdown. Power from the unit goes to a distribution panel in the machine room where it then feeds the various system components. The panel is also equipped with a number of fire safety and automatic shutdown circuits which were designed and installed.

22. Water Chiller

A five-ton water chiller was installed elsewhere in the building and connected to the Bryant disk file for cooling purposes.

23. Air Conditioner

A fifteen-ton fan-coil unit was installed in the room to provide cooling for the system. This unit was connected to the building chilled water system. This measure, taken for reasons of economy, may have been a mistake; the building system is not well regulated and seems not to be very reliable.

24. HP2100A

This commercial minicomputer was received and attached to the CHIO I multiplexer last year. No attention was required for the unit this year other than the repair of two failures.

25. Potter Tape Unit

The Potter magnetic tape unit also continued in reliable operation. This unit, a 120 ips, 800 bpi, 9-track unit is used primarily as a back-up

medium for the disk file and for communication via files with other systems. The entire BCC tape library, a collection of about 150 tapes both in 7-track, 556 bpi and 9-track, 1600 bpi format, was copied using other machines in town onto 9-track, 800 bpi tapes.

26. Iomec Line Printer

An Iomec 200 lpm line printer was received and connected to the HP2100A. This connection required an interface between the printer and the HP. The interface was designed and built as two subunits, one at either end of a 100 foot cable linking the units.

27. Connections to the ARPA Network

Before the system was operational, the hardware was connected to the TIP in the form of four RS/232 full-duplex 110 bpi terminal connections. The system actually experienced some ARPA net use during the year, but mostly in the form of several demonstrations. A different interface was also designed to connect the CHIO directly to the IMP portion of the TIP. This connection was fabricated but not checked out at the end of the year.

28. Overall System

The equipment first ran as a system on February 26, 1973. Initial reliability was horrible, but by the third week of March it had improved to the point at which we were able to guarantee four hours per day operation for users of the system. The only users permitted on the system so far have been Task II personnel and a few others on a demonstration basis only. The remaining time during the day was used for further hardware work and/or operating system development. During June

and July the system was used all day for users. Little hardware work on the system was done during this period in order to facilitate this use. The SPL compiling system was redone during this time. The system was taken out of service during the month of August for hardware catch-up work. During this time, most of the programmers took vacation. Reliability of the system over the year was not especially good, although much software work was accomplished. Most of the unreliability centered in the FM and MPMBM connections, the protects, and the Ampex core modules. Many changes were made in August which should have the effect of enhancing reliability.

B. Hardware Documentation

The state of all hardware documentation is good. Our procedure requires that all construction work be carried out at least from logic diagrams if not actual assembly drawings. Thus original drawings exist that are almost accurate. The slight changes which occur during subsequent debugging activities are shown on a copy of record which is kept in the machine room with the equipment. These changes will be reflected on the originals by maintenance personnel later during moments of lighter duties. During the period all microcode was verified and reconciled on old copies of record. Several existing microcode errors were located by this means. Then the microcode source language for every processor was updated and recompiled. Finally the recompiled microcode was checked against the copies of record and against the actual microcode boards themselves. Also during the period a wirelisting program written for the Xerox 940 was obtained from Xerox PARC and modified slightly to work with BCC-style backpanels. This program was

then used to generate up-to-date wirelists for the processors. In particular, a wirelist for the new Fast Memory backpanel was generated, converted into instructions for a Gardner-Denver wirewrap machine, and converted into punched cards for transmission to a vendor. At the end of the year, the new backpanel had not yet been received.

C. Software

The state of the operating system as received from BCC was relatively good. The system was interim and heavily patched; but its bugs had been mostly located and the patches were documented. Thus after a modest effort to find the portions of the software scattered on various tapes, collect them together, and remake the various patches, the system was ready to run well but for hardware errors. As the hardware progressed so did the operation of the system. A few new software errors were discovered and patched. The primary software accomplishment was the production of an operating SPL compiling system. The compiler originally used by BCC was written to run on the Xerox 940 and -- while thus also runnable on the BCC 500 -- ran with great inefficiency. This compiler had been written at BCC in QSPL, a 940 language. An SPL written in its own language had been almost completed but had never been debugged or documented. Production of the SPL first required checking and documenting of about 400 pages of listing. A large number of errors were found and corrected in this work. The code generator had to be written from scratch. Then compiling and on-line debugging began. Finally as a partial check on the correct operation of the compiler, it was demonstrated that it will correctly compile itself. The SPL was then used to recompile and modify a number of BCC 500 software packages. The final version contains about

20,000 source language statements.

The system utility was enhanced to provide a number of new features such as terminal linking. This required concurrent microcode changes, as the original microcode was in error. Other utility subsystems were recompiled and updated, such as a subsystem permitting use of the magnetic tape and implementing a stand-alone file system for the disk file which is almost impervious to system crashes. A number of 940 subsystems were also operational at the end of the year; these required no effort since the CPU has a 940 mode and execute 940 user code directly. These subsystems include a comprehensive text editor, a macro assembler for the 940 and interactive DDT, an interactive SNOBOL IV, a JOSS-like interactive programming language called CAL, and others.

D. NCP Activities

During the year an NCP for the BCC 500 was written entirely in microcode. Consideration was given to whether the NCP should be placed in the CHIO processor or given over to a processor of its own. It was decided to place the NCP in the CHIO, but to do so would have involved the construction of a number of microcode boards and the removal of a section of current microcode which implements the CTP and which is used heavily for system maintainance purposes. The alternative chosen was to run the NCP as a concurrent task on the CTP and allow it to call microcoded routines to facilitate its interaction with the CHIO. To do so required a choice of means by which the CTP and CHIO could time-share the same processor structure.

It was decided to write the NCP as a sequence of small tasks which could be run each to completion without interruption. Each task had to be small

enough to execute within a one-millisecond period such that the CHIO microcode could fulfill its real-time obligations. Between each task, then, the existing CHIO microcode would run as before. The NCP was written in QSPL, a self-documenting high-level language which compiles CTP code. The NCP was not actually compiled or implemented at the end of the year because of the prior necessity for installation of a private memory of the CHIO. Necessary core modules are on hand, but some hardware preparation is necessary.

The NCP contains also a TELNET. Theoretically, the NCP/TELNET code running on a CTP processor could be wheeled up next to an existing computer system and used to connect it to the ARPA network. This is not actually suggested at this time, as there are many better candidates for processors.

Effort Relating to Other Systems

A. New Microprocessor Design

In response to needs felt by NASA/Ames IAC a pilot study was launched in May to determine the feasibility of redesigning (more accurately, repackaging) the BCC standard microprocessor for use in the ILLIAC IV system. The IAC system design calls for the use of a number of small processors to perform system management functions similar to the BCC 500's CHIO, AMC, and MSCH functions. The PDP-11 was chosen for this application, but as development has progressed it has become apparent that the PDP-11 is not sufficiently powerful. The notion is to borrow technology now used on the 500: to use the processor microcode directly for implementation of frequently-called, fixed functions and to use a standard emulated CPU to run classical software more readily changed. The addition of a function call instruction allows the processor to escape from emulation to direct microcode execution of the other-

wise high-overhead functions. Other approaches are possible such as the small, uninterruptible task structure mentioned in D above. The main point is that by enhancing a, say PDP-11, with direct microcode capability of the class of the 500's microprocessor, its power can be greatly increased while maintaining its basic character as a PDP-11.

The study required about six man-months of effort and resulted in the conclusion that such a processor can be produced easily using available packaging schemes and MSI logic. Its cost is not known at this time. At the end of the year there existed almost complete logic diagrams for the processor and a section of logic called RAID (Remote Assistance In Debugging) which permits another PDP-11 to be connected to the processor via its UNIBUS and to perform almost complete hardware diagnostics. The RAID capability is of novel design and looks quite promising as a means for finding almost any type of processor failure.

B. Participation in COTCO Study

The Task was asked in July by NASA/Ames IAC to do a study on the proposed COTCO experiment. Considerable effort was expended over a short period, and a draft report was submitted to IAC in August.

C. Other Activities

Personnel from the Task attended a number of conferences. The Task sent Mr. Wrenwick K. Lee to the ARPA Graduate Student Conference. Mr. John Davidson attended a TELNET meeting and participated in the specification of the TELNET RCTE (remote-controlled echoing) option.

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DOD IMPLICATIONS

The ALOHA Radio Network of Task I serves as a prototype for the Packet Radio Group, whose objectives are to develop an experimental network which might be applied to military tactical communications.

The BCC 500 Multiprocessor of Task II is now being employed in a study of secure computer systems which has obvious ramifications for military applications.

During 1973, personnel of both Tasks have met and consulted with communications and computer specialists of CINCPAC to assist them in developing their requirements and planning for military communications in the Pacific Area. In particular we have assisted CINCPAC in planning for COTCO (Consolidation of Telecommunications in Oahu).

Plans for Further Research

In 1974 Task I plans to continue the satellite experiments on ATS-1.

It plans to further improve the repeater and TCU design with added micro-processor capability.

It plans to assist the Packet Radio Group in system design and measurements.

It plans to explore further applications where multi-access radio communications might prove beneficial.

In 1974, Task II will concentrate principally on system security issues with a specific goal of securing the TENEX operating system for the ILLIAC IV computer system.

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